REMARKS

Claims 1-16 are pending in the application. Claims 1-16 are rejected.

Claims 1, 2, 8 and 13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Titchener in view of Kawazoe et al. (Kawazoe).

It is respectfully submitted that neither references teaches or suggests the operating-object holding means sequentially holding each word respectively consisting of plural bits of transmission information, and divided into constant word lengths, in combination with the recited features of the argument holding means and operation means. Claim 2 similarly recites sequentially holding each word respectively consisting of plural bits of received series, and divided into constant word lengths.

The Office Action points to col. 46, lines 40-43 of Titchener. However by reading the next several lines in this reference it is clear that this is different from applicant's claimed invention. Col. 46, lines 40-48 of Titchener describe "transferring the least significant bit from the fixed length code to the variable length code..."

This is different from applicant's claimed invention where the operating-object holding means sequentially holding each word and argument holding means for holding an argument that should be applied to an operation that is performed on a word that is subsequently held by said operating-object holding means.

Further in applicant's operating-object holding means it is fed by being divided into units of constant word lengths consisting of plural bits, respectively. In the process of a logical operation to achieve coding or decoding, the word is supplied to operation means through argument holding means when needed.

In the Office Action it is submitted that three different sections of Titchener are being picked and chosen from to fit the operating-object holding means. This is improper because first the Office Action points to col. 45, lines 12-13 where Titchener describes the buffer means for each selected input code, then points to col. 46, lines 40-43 which describes a different input buffer means, then the Office Action points to col. 41 for the argument holding means for holding an argument that should be applied to an operation that is performed on a word that is subsequently held by said operating-object holding means, however in this section Titchener never suggest the operating-holding means sequentially holding each word respectively consisting of plural bits of transmission information, and divided into constant word lengths.

It is respectfully submitted that this rejection is improper since the Office Action is picking and choosing unrelated pieces from the Titchener reference and the different sections of the reference being pieced together purporting to show applicant's claimed feature.

In addition the Office Action admits that Titchener fails to teach the logical operation on a combination of logic values. The Office Action asserts that Kawazoe teaches simple convolutional encoder and encoder of arbitrary length.

Kawazoe teaches these type of words are input a bit at a time, and becomes an operating object of a logical operation repeatedly over a number of times (the number of times being the same number as the number of stages in the shift register.

Additionally the argument in Kawazoe, which is a part or all of the results of the preceding logical operation performed, will never be an object of a subsequent logical operation.

In addition, the word thus being held in the operating-object holding means is never updated until a subsequent word which includes subsequent bits shorter than those constituting the above constant word lengths is determined, even when the subsequent bits are to be

sequentially determined. This is clear from the description in claims 1 and 2 of the present invention, that is, "sequentially holding each word respectively consisting of plural bits of received series, and divided into constant word lengths".

In the Office Action it's also argued that it would have been obvious to make such a combination of Titchener in view of Kawazoe. However it is respectfully submitted that one skilled in the art would have found no motivation to make such a combination. There is no suggestion in the references themselves nor is there any motivation provided in the Office Action. The Office Action only states that it would have been obvious. The applicant is not provided with any reference or indication as to what makes this obvious in order to judge the assertion of the Examiner.

It is respectfully submitted that none of Titchener or Kawazoe indicate or suggest to make such a combination of references as proposed by the Office Action. It is well-established that a combination of limitations, some of which separately may be known, may be a new combination of limitations which is nonobvious under the condition of 35 U.S.C. 103. Moreover, "an examiner may often find every element of a claimed invention in the prior art." In re Rouffet, 47 USPQ3d 1453, 1457 (Fed. Cir. 1998) (reversing PTO obviousness rejection based on lack of suggestion or motivation to combine reference).

Therefore even if every element of a claimed invention is in the combined prior art there must be some suggestion or motivation to combine the references. "Although a reference need not expressly teach that the disclosure contained therein should be combined with another, the showing of combinability, in whatever form must nevertheless be 'clear and particularity.'" In re Dembiscak, 175 F.3d 994, 999 (CAFC 1999).

The only such suggestion provided has been from applicant's own disclosure.

In addition to the above reasons it is submitted that applicant's operation means never retries the logical operation until a subsequent word is supplied. As pointed out above applicant claims "sequentially holding each word respectively consisting of plural bits of received series, and divided into constant word lengths" and "holding an argument that should be applied to an operation that is performed on a word that is subsequently held by said operating-object holding means" and "performing, as said operation, in accordance with logical values of individual bits that are included in said word being held by said operating-object holding means and said argument being held by said argument holding means, coding that is defined as a logical operation to be performed on a combination of said logical values."

The results of these logical operations indicate direct results of desired coding and decoding.

In Kawazoe the object of logical operation is changed even in the process of determining such subsequent word, or since the logical operation is performed on the assumption that its object could make such changes, the invention in Kawazoe indispensably requires a complex hardware. The complex hardware must perform additional control operations such as synchronization or the like to properly obtain a result of the convolutional coding, as described in column 5, lines 59-61 in Kawazoe et al. that "upon each 3-bit addition of the original data D, the 4-bit (I_1, I_2, Q_1, Q_3) convolutional code is output".

The configurations of the inventions in claims 1 and 2 are essentially different from the configuration of the invention in the combination of the two references on the following points.

Neither an object being subjected to a logical operation nor an argument being applied to a subsequent logical operation is supplied as: a word which is added a bit being fed

subsequently; or a word which includes a part of the operation object or the argument, and a bit subsequent to the part.

In addition, the present invention can achieve results of the logical operation that the invention in the combination of Titchener and Kawazoe cannot achieve. The present invention can achieve such results of the logical operation through a normal process, whereas the invention in the combination of the three references can only achieve the same results by performing additional processes. The result of the normal process in the present invention is based on the following conditions.

- The object of the logical operation is fed, being divided into constant word lengths respectively consisting of plural bits, thereby consisting of a collection of only valid bits.

- According to the result thereby obtained in advance based on the operation object, the argument to be referred to in the process of the subsequent logical operation also consists of the collection of only valid bits.

It is respectfully submitted that at least the forgoing differences between the cited references and the present invention, claims 1 and 2, would not have been obvious in view of such a proposed combination.. Claims 8 and 13 depend on claims 1 and 2 and are likewise allowable for at least the foregoing reasons and because each claim includes additional distinguishing features.

Claims 3, 4, 6, 7, 9, 11, 12 and 14 are rejected under 35 U.S.C.§103(a) as being unpatentable over Titchener in view of Kawazoe and further in view of Lan et al. Claims 5 and 10 are also rejected as unpatentable under Titchener and Kawazoe and further in view of Kindred et al.

Claims 3-7, 9-12 and 14 depend on either of claims 1 and 2 and are likewise allowable for at least the foregoing reasons and because each claim includes additional distinguishing features.

Claims 15 and 16 are under 35 U.S.C. § 103(a) as being unpatentable over Titchener in view of Kawazoe et al. and Astrachan. However, for at least the foregoing reasons and because each claim includes additional distinguishing features the inventions in claims 15 and 16 are essentially different in their configurations from the combination of Titchener, Kawazoe et al., and Astrachan. Moreover, none of Titchener, Kawazoe et al., and Astrachan suggest such a combination of references as proposed in the Office Action.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,

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Docket No.: FUJX 17.182 (100794-11392)
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